Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.058”**

**PAD FUNCTION:**

1. **N. MR**
2. **CP**
3. **P0**
4. **P1**
5. **P2**
6. **P3**
7. **PE**
8. **GND**
9. **N. SPE**
10. **TE**
11. **Q3**
12. **Q2**
13. **Q1**
14. **Q0**
15. **TC**
16. **VCC**

**14**

**13**

**12**

**11**

**7 8 9 10**

**4**

**5**

**6**

**3 2 1 16 15**

**MASK**

**REF**

**.078”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: VCC or ISOLATED**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .058” X .078” DATE: 11/14/22**

**MFG: TIH THICKNESS .000” P/N: 54HCT163**

**DG 10.1.2**

#### Rev B, 7/1